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Docket: 0756-0864

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
Yasuhiko TAKEMURA	)	
Serial No. 08/051,313	)	Art Unit: 2515
Filed: April 23, 1993	)	Examiner: T. Duong
For: ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 9-13-96.

Rose M Fiorentino

TRANSMISSION OF CERTIFIED TRANSLATION

Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

Further to the amendment filed September 12, 1996, and to perfect applicant's claim for priority under 35 U.S.C. § 119, submitted herewith is a certified translation of Japanese Patent Application No. 4-135865, filed April 28, 1992. In view thereof, it is respectfully submitted that the outstanding rejection based on U.S. Patent 5,463,483 has

been overcome and reconsideration is requested. If the Examiner has any further questions concerning this matter, he is invited to contact the undersigned.

Respectfully submitted,

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Docket No. 0756-1264

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
YASUHIKO TAKEMURA	)	
Serial No. 08/460,687	)	Examiner T. DUONG
Filed: February 22, 1994	)	Art Unit No. 1104
For: ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME	)	

VERIFICATION OF TRANSLATION

Honorable commissioner of patents and Trademarks

Washington, D.C. 20231

Sir:

I, Kunitaka Yamamoto, Flat SEL-A 202 304-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan declare:

that I am well acquainted with both the Japanese and English Languages; and

that to the best of my knowledge and belief the following is a true and correct translation of Japanese Patent Application No. 4-135865 filed on April 28, 1992.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false

statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 10th day of May, 1996

Name: Kunitaka Yamamoto

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[Identification Number] P002096-02

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[Addressee] Director-General of patent office

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[Title of the Invention]
Active matrix display device and method of driving the same

[Number of Claims] 11

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[Name of Article]	Specification	1
[Name of Article]	Drawing	1
[Name of Article]	Abstract	1

[Name of Document] Specification

[Title of the Invention]

ACTIVE MATRIX DISPLAY DEVICE AND METHOD OF DRIVING THE SAME

[Claim]

[Claim 1] An active matrix display device wherein an active matrix static display device has at least one TFT to each picture-element which has a gate electrode connected to a gate line (a first gate line) and a picture-element electrode connecting either a source or a drain to a data line, where said picture-element electrode is formed over the first gate line with an insulator provided therebetween, and also over a gate line other than the first gate line or a wiring running parallel to the first gate line with an insulator provided therebetween.

[Claim 2] The display device of claim 1 wherein the difference between overlapping area of said picture-element electrode and said first gate line, and the overlapping area of said picture-element electrode and said gate line other than the first gate line or the wiring running parallel to the first gate line is 1/10 or less of the sum of said two areas.

[Claim 3] An active matrix display device driving method wherein antiphase voltage is applied to a wiring running parallel to a gate line while a pulse is being applied to the gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over the gate line with an insulator provided therebetween, at the same time, formed also oyer said wiring running parallel to said gate line with an insulator provided therebetween.

[Claim 4] An active matrix display device driving method wherein antiphase voltage is applied to a wiring running parallel to a gate line

while a pulse is being applied to the gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over the wiring running parallel to the gate line with an insulator provided therebetween.

[Claim 5] An active matrix display device driving method wherein antiphase voltage is applied to a gate line (a second gate line) other than a first gate line while a pulse is being applied to the first gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over the first gate line with an insulator provided therebetween, at the same time, formed also over the second gate line with an insulator provided therebetween.

[Claim 6] An active matrix display device driving method wherein antiphase voltage is applied to a gate line (a second gate line) other than a first gate line while a pulse is being applied to the first gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over the second gate line with an insulator provided therebetween.

[Claim 7] An active matrix display device driving method wherein a bipolar pulse which is a combination of two pulses, with opposite polarities is applied to a fist gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over the first gate line with an insulator

provided therebetween, at the same time, formed also over a gate line (a second gate line) other than the first gate line with an insulator provided therebetween.

[Claim 8] An active matrix display device driving method wherein a bipolar pulse which is a combination of two pulses with opposite polarities is applied to a fist gate line, where the display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and the picture-element electrode is formed over a gate line (a second gate line) other than the first gate line with an insulator provided therebetween.

[Claim 9] An active matrix display device wherein a picture-element at a row (n) and a column (m) and another picture-element at a row (n+1) and the column (m) are located opposite to each other with a data line (m) running inbetween, where the active matrix display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line.

[Claim 10] An active matrix display device wherein the polarity of a signal sent to a first data line and that to a second data line are opposite, where the active matrix display device has at least one TFT to each picture-element which has a gate electrode connected to the gate line and a picture-element electrode connecting either the source or drain of the TFT to a data line, and has a structure where the picture-element electrode is arranged between the first data line and the second data line which is located next to the first data line.

[Claim 11] An active matrix display device having at least one TFT to each picture-element which has a gate electrode connected to a first gate line and a picture-element electrode connecting either the source or

drain of the TFT to a first data line, and the picture-element electrode has substantially the same shape as the area surrounded by a first data line, a second data line which is located next to the first data line, a first gate line and a second gate line which is located next to the first gate line.

[Detailed Description of the Invention]

[0001]

[Field for Industrial Use]

The present invention relates to a static display device such as a liquid crystal display device, especially a display device having an active matrix.

[0002]

[Prior Art]

During recent years, an active matrix circuit for driving a liquid crystal display has been actively studied and put into practical use. As for an active element, the use of a thin film transistor (TFT) with one conductivity-type for a picture-element has been proposed. Such an active matrix circuit is comprised of capacitors, each constituted by a picture-element electrode, a counter electrode and liquid crystal interposed between foregoing electrodes. Incoming/outgoing charges to/from a capacitor are controlled by a TFT. In order to display stable images, the voltages at both electrodes of each capacitor are required to be kept constant, however, it has been difficult for some reasons.

[0003]

The most significant reason is that charges leak from the capacitor even when the TFT is in an off-state. There is another leakage of charges inside of the capacitor, however, the former leakage of the charges from the TFT is larger than the latter leakage by about one order. When this leakage occurs intensively, there occurs a phenomenon, so-called flicker that brightness of an image is varied at the same frequency as a frame frequency. Another reason is the variation of a voltage (Δ V) which is

induced by a capacitance coupling of a gate signal to a picture-element potential due to a parasitic capacitance between a gate electrode of the TFT and the picture-element electrode.

[0004]

In order to solve these problems, an auxiliary capacitance (or additive capacitance) has been disposed in parallel to the picture-element capacitance. Provision of such an auxiliary capacitance causes a time constant of discharging of charges from the picture-element capacitance to be increased. In addition, when a gate pulse (signal voltage) is represented by V_G, the picture-element capacitance by C_{LC}, the auxiliary capacitance by C, and the parasitic capacitance between the gate electrode and the picture-element electrode by C', ΔV is given by;

$$\Delta V = C' V_G / (C_{LC} + C' + C)$$

and ΔV can be reduced if C is larger than C' and C_{LC}.

[0005]

[Problems to be Solved by the Invention]

Conventionally, a circuit construction as shown in Fig. 2(A) or 2(B) has been adopted for the auxiliary capacitance. These circuit arrangements are shown by circuit diagrams of Fig. 2(C) and 2(D), respectively. In Fig. 2(B), a ground line, for example $X_{n'}$, is formed in parallel to a gate line X_n (or data line Y_m), and a picture-element electrode is formed so as to be overlapped with the ground line, thereby forming a capacitance C. In Fig. 2(B), the auxiliary capacitance C is represented by a shaded area, and C_{LC} represents a picture-element electrode. However, in this method, an additional wiring has to be formed, causing a smaller aperture ratio and a darker screen.

[00006]

On the other hand, an arrangement shown in Fig. 2(A) wherein a picture-element electrode which is connected to the gate line X_n is partially overlapped with a next gate line X_{n+1} to form an auxiliary capacitance C (as indicated by a shaded area) at the overlapping area, is

proposed. In this method, an additional wiring is not formed, thus the aperture ratio is not lessened. However, it has been known that a gate pulse is affected by a capacitance added to the gate line.

[0007]

At any rate, these methods are not substantial solutions particularly to Δ V. These methods provide some degree of effect in a point that the time constant of the discharging of the picture element is lengthened. however, no solution has been made to the point that Δ V occurs asymmetrically. Fig. 3(C) shows a driving operation of a conventional TFT active matrix circuit. In this case the potential of a counter electrode of a picture-element is set to "0" V, and the potential of the gate line at non-selection time is also set to "0" V. However, as usually adopted, the potential of a counter electrode may be added with a proper offset potential while the potential of the data line is also added with the same offset potential. Actually, the same result as shown in Fig. 3 is obtained. Particularly when the potential of the gate line and the potential of the counter electrode are set to zero as shown in Fig. 3, the signal of the data line is required not to exceed a threshold voltage of the TFT, and no stable matrix driving can be performed unless this condition is satisfied.

[0008]

As is apparent from the figure, Δ V shifts down its electric potential with respect to the data signal. For example, even when an auxiliary capacitance is added to reduce Δ V, the response is still asymmetrical. In this point, the provision of the auxiliary capacitance is a passive countermeasure. The present invention is made with the consideration of the above points, and based on the completely different idea from that of conventional methods. The object of the present invention is to reduce Δ V with more drastic measure, and to propose a satisfying display method and display device for that purpose, more particularly, provision of effective arrangements of picture-elements and circuits of a display device.

[0009]

[Measures to Solve the Problems]

ΔV is originally caused by the application of a pulse only to the gate electrode. If, in addition to a first TFT, the same type of second TFT having the same amount of parasitic capacitance as the first TFT is added in a picture element, and a pulse having a different polarity and the same height of a gate pulse is applied to the second TFT simultaneously with the application of the gate pulse, the contribution of the gate pulse to a picture-element electrode could be offset. The inventor of this application has found this technical idea, and further developed the theory. As a result, it was found that the same effect can be obtained without providing the additional second TFT if a circuit having the equivalently same capacitance is provided.

[0010]

That is, when a parasitic capacitance between a gate electrode and a picture-element electrode is represented by C_1, a parasitic capacitance between a second wiring other than the gate electrode and the picture-element electrode by C2, the height of a pulse of the gate electrode by V_1, and the pulse height of the second wiring by V_2, ΔV is given by;

$$\Delta V=-(C_1V_1+C_2V_2)/(C_1+C_2)$$

If $V_2=0$, the data signal would be lowered by ΔV like the prior art. However, when $V_2=-C_1V_1/C_2$ is satisfied, ΔV would be equal to zero. For example, when $C_1=C_2$, ΔV is mutually counteracted to be zero if $V_2=-V_1$. As described above, in comparison with the conventional method wherein an auxiliary capacitance is provided to relatively reduce ΔV, the method of the present invention is a more active method wherein an increase of voltage is generated to counteract with ΔV thereby offsetting ΔV.

[0011]

According to further consideration of the inventor, the following matter has been also found. Even when the gate pulse and the pulse of the

second wiring are not completely synchronized, if the device is so designed that the pulse of the second wiring is dropped after the gate pulse is dropped, the same effect as that of the case the both are completely synchronized, is obtained, although the potential of the picture-element electrode may temporarily varied. The pulse starting time for the gate pulse may be earlier or later than that of the second-wiring pulse because ΔV occurs at the off-time of the gate pulse.

[0012]

As for the second wiring, a line can be provided separately or another gate line can be utilized. By further extending the idea, it has been found that even when a gate line for driving said picture-element is overlapped with the picture-element electrode, there won't be any problems, in the present invention, as long as the second wiring can provide the same capacitance as that of the overlapping area. The capacitance formed through the above is rather effective since it acts as an auxiliary capacitance to increase the time constant of the picture element.

[0013]

This means that a slight amount of parasitic capacitance of a TFT does not cause a problem as long as it is considered as one of design factors. With the conventional method (Fig. 2), nobody dared to adopt such a design that a picture-element electrode is overlapped with a gate line for driving the picture-element because this design remarkably increases parasitic capacitance. The present invention is an epoch-making invention which breaks this long-continued-custom. As described later, the above design of this invention is ideal in improving aperture ratio. This is because the picture-element electrode is formed as far away as possible from the TFT and the gate line since the prior art concerns about the problem of parasitic capacitance between the gate electrode/line and the picture-element electrode, thus, dead spaces were considerably large. Particularly when an area assigned to one picture element is reduced, the aperture ratio tends to be reduced also.

[0014]

In a case where the gate pulse and the pulse of the second wiring are designed so as to have the same pulse height (but opposite polarities), a permissible range for C_1 and C_2 is calculated. Considering a case where the picture-element electrode is very small, the capacitance of the picture element itself is very small. On the other hand, it is technically difficult to reduce the size of the TFT, and thus the parasitic capacitance would be invariable. Even if the auxiliary capacitance is provided as a countermeasure like the prior art, the ratio of the auxiliary capacitance to the parasitic capacitance is about 10:1. If this invention is applied to obtain the same effect, the sum of C_1 and C_2 (parasitic capacitance of the TFT is included in C_1 or C_2) is required to be as large as ten times or more of the difference between C_1 and C_2. And achieving this requirement is relatively easy.

[0015]

The above case corresponds to a case where the ratio of C_1:C_2 is made close to 1:1, however, there are certain cases where it is easier to set the ratio for the C_1:C_2 close to another ratio. In such a case, the minimum amount of ΔV is generated by controlling the ratio between V_1 and V_2. For example, when C_1:C_2=1:2, then V_1:V_2=2:-1.

[0016]

For example, even when the circuit construction is identical to that of the prior art as shown in Fig. 2, the voltage satisfying the condition of this invention may be applied to a gate line (X_{n+1}) and a ground line (X_n) which do not participate in the driving of said picture element. The parasitic capacitance is considerably large in amorphous TFTs or the like to which a self alignment system is not applicable; however the deviation thereof can be controlled with high accuracy, for example, within 10%. This value of the parasitic capacitance is represented by C_1. It is possible to form an auxiliary capacitance C_2 which has the capacity as large as five times of that of C_1, with high controllability by a

geometrical method. In this case, if an insulating film of a capacitor is designed in the same thickness, the auxiliary capacitance can probably be formed with accuracy within 1%. In the conventional method, ΔV is given by $\Delta V=(0.17\pm 0.017)V_1$. However, if the present invention is applied and V_2 is set to be equal to $-0.2V_1$, ΔV is given by $\Delta V=\pm 0.017V_1$. The application of the present invention method does not improve the deviation of ΔV, however, the magnitude of ΔV is reduced down to one-tenth or less (zero in average) of that in the conventional method.

[0017]

In the above description, the signal to be applied to the second wiring is required to have the opposite polarity of the gate pulse. This means not only that if the gate pulse is positive, the second signal is negative. The optimum pulse height of a signal to be applied to the second wiring is the sum of the potential of the second wiring at the non-selection time and the potential $-C_1V_1/C_2$. The opposite polarity, in this invention, means that the potential of the signal to be applied to the second wiring is shifted in the opposite direction of the direction the potential of the gate pulse shifts. Accordingly, for example, when the potentials of the gate at the non-selection time and the second wiring are set to 0V and 10V, and the potential of the gate line at a selection time is set at 8V, the potential of the second wiring is required to be 10V or less, however, it is not necessarily required to be negative.

[0018]

The circuit construction with which the present invention is implemented is shown by Figs. 1 (A) and (B). Here, C_1 and C_2 are both capacitances obtained through overlapping a wiring and a picture-element electrode. In both circuit constructions, the gate line to drive subject picture element is overlapped with the picture-element electrode.

[0019]

In Fig. 1 (A), exclusive wirings $X_{n'}$ and $X_{n+1'}$ are provided independently of the gate lines X_n and X_{n+1}. If pulses with the opposite polarities and the same height are to be applied to X_n and $X_{n'}$, C_1 and C_2 are required to be formed as equally as possible. Fig. 1 (C) is a circuit diagram of Fig. 1 (A).

[0020]

In Fig. 1 (B), capacitance C_1 and C_2 are formed through overlapping a gate line (X_n) which drives subject picture element and a gate line in the next row (X_{n+1}) with a picture electrode. In this case also, of course, C_1 and C_2 are required to be formed as equally as possible if pulses with the opposite polarities and the same height are to be applied almost simultaneously to X_n and X_{n+1}. In this case, it is preferred to arrange them alternately as shown in the figure to utilize the area effectively. Such an alternate arrangement is convenient also for a color-arrangement of picture elements.

[0021]

That is, in the prior art, picture elements have been arranged in a honeycomb shape or hexagonal shape to improve a color mixing. In such a case, wirings are bent in accordance with an arrangement shape of the picture elements. That increases wiring resistance and causes the increase of fraction defective due to difficulty in manufacturing. In the present invention on the other hand, an ideal hexagonal structure can be obtained without bending the wirings.

[0022]

A circuit diagram of Fig. 1 (B) is shown by Fig. 1 (D). In this case, a bipolar pulse which is a combination of a positive pulse and a negative pulse is required to be applied to the gate line. This is because when one gate line is being selected, the other gate line is required to be supplied with a voltage having opposite polarity. The voltage to a picture element $Z_{n,m}$ is temporarily affected by a pulse applied to C_2 for driving a picture element $Z_{n+1,m}$.

[0023]

The operations of these circuits are shown in Figs. 3 (A) and (B). Fig. 3 (A) shows an example of the driving operation of the circuit shown in Figs. 1 (A) and (C), and Fig. 3 (B) shows an example of the driving operation of the circuit shown in Figs. 1 (B) and (D). In a case where there is a time lag between a pulse which is applied to drive the subject picture element (TFT) and a pulse which is applied to cancel ΔV, the voltage is temporarily varied, but soon returned to its original state. Therefore, the influence of such a variation of the voltage is very slight, and thus it is visually unidentifiable.

[0024]

For forming such circuits, conventional TFT fabrication techniques can be directly adopted. And more favorable fact is that since no attention is required to the parasitic capacity between a gate line and a picture-element electrode unlike the prior art, a number of processes can be reduced with a back-surface exposure technique using metal wiring as a mask. Fig. 4 shows an example of the circuit thus formed. As shown in the figure, a picture-element electrode 412 is partitioned by metal wirings, that is, a gate line 402 and a data line 408. However, the picture-element electrode and the metal wirings are geometrically overlapped due to diffraction of light in an exposure process. As apparent from the explanation heretofore, the overlapping area of the picture element and the gate line will not cause a problem.

[0025]

There will be no problem also with the overlapping area of the picture element and the data line. Of course it cannot be denied that a signal to the data line continuously leaks to the subject picture element, causes noise, and induces a phenomenon so-called cross-talk. However, the extent of the problem can be sufficiently minimized. For example, reducing the spacing between the gate lines so that the capacitance generated by the overlapping area of the data line and the picture-element electrode is made smaller in comparison with the auxiliary

capacitance C_1 and C_2.

[0026]

The cross-talk phenomenon can be further suppressed by alternating every other data line. For example, when a positive signal, in comparison with the counter electrode of the picture element, is applied to a data line Y_m, a negative signal, in comparison with the counter electrode of the picture element, is applied to a data line Y_{m+1}, in other words, reversing the polarity of the signal to Y_{m+1} from that to Y_m. Of course, video signals to be applied to the respective data lines are independent of one another, however, it can be regarded that substantially same video signals are sent to these data lines because the video signals of the neighboring picture elements are similar to one another. Therefore, the signals to be applied to the data lines Y_m and Y_{m+1} have the same pulse height and opposite polarities, thus these signals mutually offsets to cease the influence to the picture-element electrode. As a result, cross-talk induced by the coupling between the data line and the picture-element electrode no longer occurs.

[0027]

Fig. 5 indicates an embodiment of such a picture element and TFT fabrication processes. In this embodiment, a reverse stagger type which is used for an amorphous silicon TFT is formed. However, the same back-surface exposure technique can be used for a planar type.

[0028]

First, a gate line 402 is formed on a substrate 401, and an oxide 403 is formed on the surface of the gate line 402 by an anode-oxidation method if occasion demands. Thereafter, a gate insulating film 404 is formed, a semiconductor channel region 405, a drain region 406 and a source region 404, and a data line 408 is formed (Fig. 5 (A)). Then an insulating planarizing film 409 of polyimide or the like is formed, and an electrode hole is made in the insulating planarizing film. Thereafter, a transparent conductive film 410 is formed at the front surface, and a

photoresist is coated on the front surface (Fig. 5 (B)). The same method as the conventional TFT fabrication method is used, up to this point.

[0029]

Next, light is irradiated from the back side of the substrate to expose the resist to light. In this case, the wavelength of the light and thickness of the semiconductor regions 406 and 407 are preferably so controlled that the light can pass through the semiconductor regions. Consequently, the resist at the metal wiring portion is removed, and only the resist 411 at the other portion remains. Of course, a part of the resist on the metal wirings remains due to diffraction of the light. These processes are shown in Fig. 5 (C).

[0030]

Finally, the transparent conductive film is etched using the residual resist as a mask to form a picture-element electrode 412 overlapped on the gate line 402. In the above process, a mask positioning operation which has been conventionally required in the etching process of the transparent conductive film becomes unnecessary. Particularly in a case where the mask positioning is carried out and the transparent conductive film is etched, it has been difficult to precisely control the sizes of C_1 and C_2 due to the deviation of the mask. In the present method, on the other hand, the sizes of C_1 and C_2 are almost equal to each other, and it is favorable for the object of the present invention. Moreover, the overlapping area of the picture-element electrode and the data line is symmetrical between the right and the left, and by properly performing the alternation of the data line as previously described, the cross-talk can be completely eliminated.

[0031]

[Embodiment 1]

Fig. 6 (A) is a top view of a circuit having an auxiliary capacitance which is formed by the method of this embodiment. This circuit is identical to that of Fig. 1 (B) in principle, and its operation is carried out in the manner as shown in Fig. 3 (B).

[0032]

In the figure, X_n to X_{n+3} represent gate lines, and Y_m and Y_{m+1} represent data lines. Two gate lines necessarily run across each picture-element electrode C_{LC}. One of the gate lines is the one to drive the picture element and constitutes a gate electrode of a TFT while the other isn't. The picture-element electrode is formed over a gate electrode (G), a source region (S), and a drain region (D) etc. of the TFT and is connected to the source region of the TFT through a contact hole. In this case, unlike the case of Fig. 1 (B), the gate electrode of the TFT does not extend into the picture element. This feature is very convenient for equalizing the capacitances C_1 and C_2.

[0033]

The TFT and the picture element may be formed using the conventional technique. For example, when a planar type of TFT is intended to be formed in a self-alignment process, a method disclosed in Japanese Patent Application No. 4-30220, No. 4-38637 or No. 3-273377 may be used.

[0034]

In this embodiment, a structure of metal wiring (aluminum)/anode-oxide (aluminum oxide)/picture-element electrode (ITO) is used as the cross-sectional structure of the auxiliary capacitances C_1 and C_2. In order to obtain this structure, a method comprising;

a process forming the gate line with aluminum,

a process forming aluminum oxide over the surface of the gate line using an anode-oxidation method, and

a process forming the picture-element electrode thereon,

may be used. In this case, aluminum oxide has dielectric constant three times as high as that of silicon oxide, and thus it can contribute to increase the auxiliary capacitance. Furthermore, when a large auxiliary capacitance is required, the gate line made of tantalum or titanium and subjected to the anode-oxidation may be used, utilizing the oxide as a dielectric body for auxiliary capacitance.

[0035]

Alternately, in place of the foregoing fabrication method and the structure, a conventionally well-used method for metal wiring/oxide (such as silicon oxide, silicon nitride, etc. which can be formed by CVD method or sputtering method)/picture-element electrode may be used instead.

[0036]

[Embodiment 2]

Fig. 6 (B) is a top view of a circuit having auxiliary capacitance which is produced by this embodiment. This circuit is also identical to that of Fig. 1 (B) in principle, and its operation is carried out by the method as shown in Fig. 3 (B).

[0037]

In the figure, X_n to X_{n+3} represent gate lines, and Y_m and Y_{m+1} represent data lines. Two gate lines necessarily run across each picture-element electrode C_{LC}. One of the gate lines is the one to drive the picture element and constitutes a gate electrode of a TFT while the other isn't. The picture-element electrode is formed on a gate electrode (G), a source region (S) and the drain region (D) of the TFT, and is connected to the source region of the TFT through a contact hole. In this case, unlike the case of Fig. 1 (B), the gate electrode of the TFT does not extend into the picture element. This feature is very convenient for equalization of the capacitances C_1 and C_2.

[0038]

In this circuit arrangement, the semiconductor regions of the two TFTs are put together. The structure has an advantage that, for example, when the data line and the semiconductor region (drain region) are contacted with each other, plural contact holes can be formed. Even when some of them are defective, the two TFTs function normally as long as at least one of the contact holes is normal. The same fabrication method and the same structure of the auxiliary capacitances C_1 and C_2 as those of the embodiment 1 are used also in this embodiment.

[0039]

[Effects]

As described above, according to the present invention, Δ V can be eliminated. There has been no attempt made to remove the influence of Δ V by such an active way before the present invention. In this regard, the present invention can be called an epoch. In addition, the present invention proposes an effective picture-element arrangement for the purpose. Such a picture-element arrangement is also effective for a color display. The embodiment heretofore explained relates to a planar type of TFT which is often used for a polysilicon TFT. However, the same effect can be obtained for a reverse stagger type of TFT which is often used for an amorphous silicon TFT.

[0040]

Furthermore, in the above description, the concrete operation method of the active matrix circuit was not described. In place of a conventional analog gradation system, a digital gradation system which was invented by the inventor of this application (for example, as disclosed in Japanese Patent Application No. 3-163873) may be adopted with no problem, whereby the gradation display can be performed using the active matrix circuit.

[Brief Description of Figures]

Fig. 1 is a diagram showing an arrangement of an active matrix circuit and its circuit diagram;

Fig. 2 is a diagram showing an arrangement of a conventional active matrix circuit and its circuit diagram;

Fig. 3 shows a driving methods for the active matrix circuits of the prior art and the present invention;

Fig. 4 shows an embodiment of the circuit arrangement of this invention;

Fig. 5 shows an embodiment of a fabrication method of the circuit of the present invention; and

Fig. 6 is a diagram showing the circuit arrangement of the active matrix

circuit of this invention.

[Description of Numbers]

401 Substrate

402 Gate Line

403 Anode Oxide

404 Gate Insulator

405 Semiconductor (Channel) Layer

406 Drain Region

407 Source Region

408 Data Line

409 Planarization Layer

410 Transparent Conductive Film

411 Photoresist

413 Picture Element Electrode

[Name of Document] Abstract

[Abstract]

[Purpose]

Reducing ΔV occurs while the off-time of a gate pulse in a static display device such as an active matrix liquid crystal display device having TFTs, and proposing an optimum arrangements for picture-element electrodes and circuits for the foregoing.

[Construction]

When C_1 is a capacitance between a gate line and a picture-element electrode, and C_2 is a capacitance of a second wiring, the potential of the second wiring is increased by C_1V_1/C_2 when a gate pulse is decreased by V_1.

[Selected Figure] Fig. 1